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MEMO CONCERNING

Driver interface v2.2

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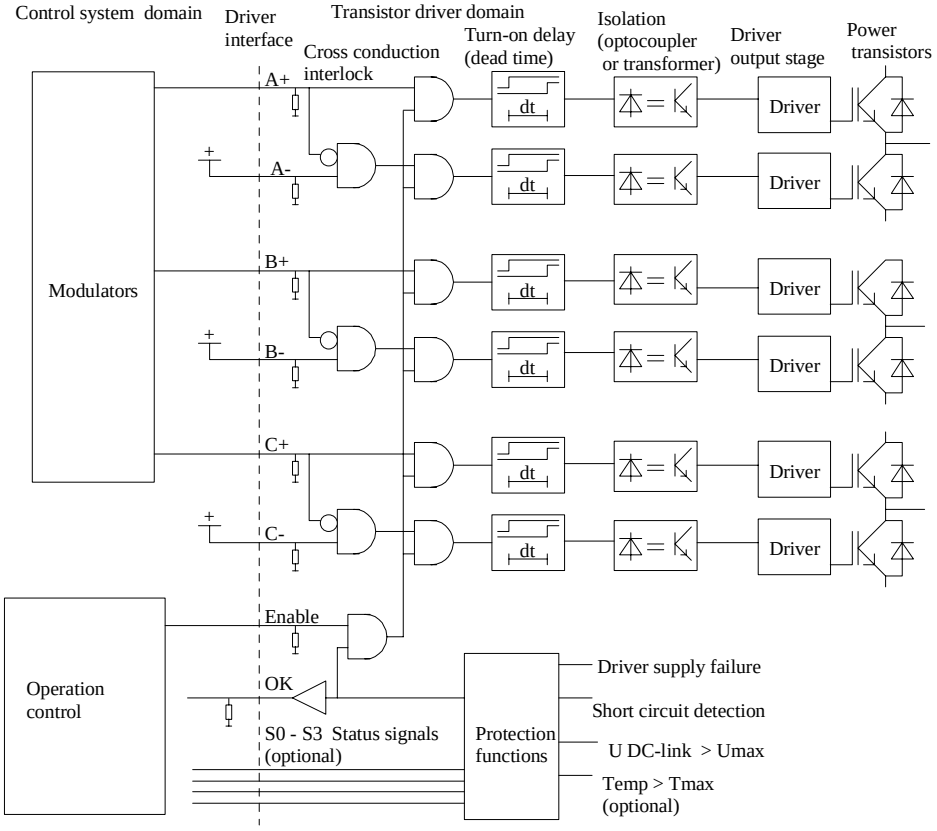
An interface for the digital signals between the transistor driver domain and the control system domain of a three phase inverter is defined. In this way all issues regarding transistor driving and bridgeleg control are confined to the transistor driver domain. Analog signals for current, voltage or temperature measurements is not covered by this definition.



Structure of digital signal interface between drivers and control system. Overview.

Structure:

- Regulators and modulators are defined to belong to the control circuit side of the interface.
- Driver circuits, galvanic isolation, dead time and cross conduction interlock circuits are defined to belong to the power circuit side.
- A global Enable signal is used to block all switching.
- Both switches in a bridgeleg can be independently controlled, but interlock logic protects against turning both bridgeleg switches on simultanously.
- ON-signal at both switches in a bridgeleg is defined to set Upper switch ON and Lower switch OFF. This can be utilized for single signal bridgeleg control.
- Failures detected by the driver system gives internal shutoff. This is reported to the control system by an OK-signal. Diagnostics information can be given by four status signal lines.

Signals:

- Signal level: 5V CMOS logic. Active high.
- Fail to safe operation is ensured by using active high logic and by using resistors to tie the signal inputs to signal ground.
- Apart from the transistor control lines, the Enable and the OK-signal lines must be present. The four status signal lines are optional.

Connectors:

- 16 pin flat cable is used for the driver interface.
- For connection beween separate boxes, 15 pin D-sub connectors are used. Pin numbering of D-sub connection is derived from D-sub contacts with press-on flat cable connction.
- Pin 1 is left unused in the flat cable. It is reserved for future use.
- MALE D-sub connector is used at for the termination at the Transistor driver side. A FEMALE D-sub connector is used at the Control system side. All cables are made as extension leads.
- A common +5V supply can be connected through pin 16 on the flat cable. When D-sub connection is used, this connection is broken. Local +5V supplies is then used. This segregation enhances the integrity of the +5V supplies.

Status signal lines, example of use:

- The status signals T0-T3 is used as hexadecimaly coded status codes.
- The status codes are sorted by priority, giving the most important condition the highest code number
- If more than one condition is present, the one with the highest number is reported. Coding can be done by using a CMOS 4532 priority encoder IC.
- The four status signal lines are defined with inverted logic. This gives all four signal lines Low for the status code number F(hex). By assigning this code for 5V power supply failure, ambiguous signalling is avoided at startup, power down, or 5 V failure conditions.

Revisions:

Jan.1990:	Version 1 introduced. Bridgeleg control only.
Jan. 1994:	Version 2 defined. Pin redefinition. Independent bridgeleg transistor control introduced.
Sept.1997:	Version. 2.1. Description is rewritten. No physical changes.
March 2000:	Version 2.2: Pin 1 is changed from Screen to n.c, Reserved.

Interface v2.1. Pin numbering:

Flatcable.	D-sub.	Signal.
1	1	n.c. (Reserved)
2	9	Signal ground.
3	2	A+ On (H). In.(Blocks A-)
4	10	A- On (H). In. (If A+ is Off)
5	3	B+ On (H). In.(Blocks B-)
6	11	B- On (H). In. (If B+ is Off)
7	4	C+ On (H). In.(Blocks C-)
8	12	C- On (H). In. (If C+ is Off)
9	5	OK-signal (H). Out.
10	13	Status code T3 (Inverted logic). Out.
11	6	Status code T2 (Inverted logic). Out.
12	14	Status code T1 (Inverted logic). Out.
13	7	Status code T0 (Inverted logic). Out.
14	15	Global enable. (H). In.
15	8	Signal ground.
16	-	+5V, Power supply. (Not D-sub.)

Status coding. Example:

OK	T3	T2	T1	T0	HEX.	Status.
L	L	L	L	L	F	+5V supply failure / Startup delay
L	L	L	L	H	E	Failure Phase A+
L	L	L	H	L	d	Failure Phase B+
L	L	L	H	H	C	Failure Phase C+
L	L	H	L	L	b	Failure Brake chopper.
L	L	H	L	H	A	Failure Phase A-
L	L	H	H	L	9	Failure Phase B-
L	L	H	H	H	8	Failure Phase C-
L	H	L	L	L	7	Signal 7
L	H	L	L	H	6	Signal 6
L	H	L	H	L	5	Signal 5
L	H	L	H	H	4	Signal 4
L	H	H	L	L	3	Overvoltage.
L	H	H	L	H	2	Signal 2
L	H	H	H	L	1	Signal 1, Main contactor open.
H	H	H	H	H	0	OK, Ready.